Shahab Ardalan

Address: One Washington Sq.
San Jose, CA, 95192
Phone: 1-408-924-4075
Email: ardalan@ieee.org
Homepage: www.engr.sjsu.edu/ardalan and www.ams.sjsu.edu

Education

Ph. D., Electronic Engineering **2003-2007**
University of Waterloo, Waterloo, Canada
Thesis: "A Novel Low-Power / High-Speed CMOS Clock and Data Recovery Circuit"

- Low-Power 5Gbps CMOS Clock and Data Recovery Circuit: Design, implementation and test of a new phase detector with novel high-speed, low-input swing CMOS D-Flip-Flops.
- A Wireless Bio-implantable Device for Monitoring Blood Pressure of Transgenic Mice: Design, implementation and test of an implantable telemetry microchip (team work, winner of "industrial award" from Strategic Microelectronics Council of Canada).
- DCML: A new ultra high speed logic circuit architecture called distributed current mode logic (DCML) has been designed. DCML is able to operate up to 60GHz in 0.13µm CMOS technology (Team work).
- Low Noise VCO: Design and implementation and test of a low substrate noise Voltage Controlled Oscillator (VCO).

M. A. Sc., Electronic Engineering **2002-2003**
Ryerson University, Toronto, Canada
Thesis: "A 1.2V, 100MHz, 8-bit Pipelined Analog-to-Digital Converter"

- Low Voltage ADC: The 100MSPS Pipelined ADC is designed and fabricated in 0.18µm CMOS technology
- CDB Logic Family: A low power technique called Current-Driven-Bulk (CDB) has been used to reduce the average propagation delay of static CMOS logic circuits in critical paths.

B. A. Sc., Electronic Engineering **1994-1999**
Amirkabir University, Tehran, Iran
Thesis: "Design, Simulation and Synthesis of a 32-bit Math-Processor with VHDL"

- Math-Processor: A 32-bit floating point Math-Processor designed with VHDL and synthesized by Synopsys. Control Unit is designed by micro controlling method with 64 micro instructions in 4 parallel fields. Synthesis result illustrates that it has more than 27000 cells.

Skill

- Signal Integrity, phase lock loop, clock and data recovery and signal conditioning (equalizer)
- Analog to digital convertors
- High speed, mixed mode system modeling and circuit design
- Low voltage, low power circuit design
- Biomedical circuit design
- Digital VLSI design (VHDL, Verilog)
- System level and behavioral modeling using MATLAB, Simulink and Verilog-A
- Computer architecture: Microprocessors, micro-controllers and DSP processors
- Experienced in using Cadence, Mentor Graphics, Synopsys, MATLAB, ModelSim, and Leonardo
- Computer programming with C++, Delphi, VBasic, Prolog, and Assembly

Teaching Experience

Assistant Professor, San Jose State University

- EE-125: Analog CMOS Integrated Circuit F12
- EE-224: High Speed CMOS Circuit S11,F11,S12,F12
- EE-227: Signal Integrity in AMS ICs S11,F11,F12
- EE-288: Data Conversions/AMS ICs S12

Adjunct Lecturer, University of Waterloo

- ECE-437: Integrated VLSI Systems Winter 2006

Short Course/Tutorials/Mentor

- Workshop, Substrate Noise Mitigation in Systems on Chip (4 Hours)
  - (cancelled due to H1N1 flu in Mexico)
  - 52nd IEEE International Midwest Symposium on Circuits and Systems, Mexico, 2009
- Short course, An Awareness of Security Aspect in Design of Digital Circuits & Systems (4 Hours)
  - 5th IEEE International Northeast Workshop on Circuits and Systems, Montreal, Canada 2007
- Tutorial, Substrate Noise Suppression Techniques for Systems on Chip (4 Hours)
  - 49th IEEE International Midwest Symposium on Circuits and Systems, Puerto Rico, 2006
- 4th Year Design Project, Mentor and Consultant, "RFID Hands-Off Temperature Sensor"
  - University of Waterloo, 2006

Publication

1. H. Goodarzi, S. Pazouki, M-R. Haghifam, **S. Ardalan**, " Comparison of different objective functions to determine optimal the location and capacity f distributed generation with uncertainty data", IEEE Electrical Power and Energy Conference, 2012, (6 pages) (accepted for publication)
2. S. Raju, **S. Ardalan**, S. Hamedi Hagh, R. Balasubramanyam, "Digital LNBC for Radio Astronomy", Collaboration for Astronomy Signal Processing and Electronics Research, 2012.
3. A.K. Zadeh, C. Gebotys, **S. Ardalan**, "Counteracting Power Analysis Attack Using Static Single-ended Logic", IEEE International Symposium on Circuits and Systems, 2011, (4 pages)
4. **S. Ardalan**, K. K. Moez, M. Sachdev, M. I. Elmasry, "Distributed Current Mode Logic," 4th IEEE Northeast Workshop on Circuit and System (NEWCAS), 2006, (4 pages)
5. M. Maymandi-Nejad, I. Lovich, **S. Ardalan**, M. Sachdev; "A Wireless Bio-Implantable Device for Monitoring Blood Pressure of Transgenic Mice," CMC Microsystems Annual Symposium, 2005, (4 pages)
6. **S. Ardalan**, D. Chen, M. Sachdev, A. Kennings, "Current Mode Sense Amplifiers," 48th IEEE Mid-West Symposium on Circuit and System, 2005, (4 pages)
7. **S. Ardalan**, A. Adibi, "Design, Simulation and Synthesis of a 32-bit Math-Processor," 48th IEEE Mid-West Symposium on Circuit and System, 2005, (4 pages)
8. D. Rennie, **S. Ardalan**, M. Sachdev, "5 Gb/s CDR Circuit with Static Phase Offset Calibration Circuit," Micronet Annual Workshop, 2005, (4 pages)

9. D. Rennie, **S. Ardalan**, M. Sachdev, "Circuit Techniques for 5 Gbit/s CDRs," Micronet Annual Workshop, 2004, (4 pages)
10. P. Mahdian, **S. Ardalan**, "Design and Implementation of a Bidirectional Interface," 3rd IEEE ICUE, 2004, (4 pages)
11. **S. Ardalan**, M. Sachdev, "An Overview of Substrate Noise Reduction Techniques," 5th IEEE International Symposium on Quality Electronic Design, 2004, (6 pages)
12. **S. Ardalan**, K. Ardalan, M. Sachdev, "A 0.8V, 8-bit, 75MSample/sec Pipelined Analog-to-Digital Converter," 46th IEEE Mid-West Symposium on Circuit and System, 2003, (4 pages)
13. **S. Ardalan**, K. Raahemifar, F. Yuan, "Low-Voltage, Low-Power Operational Amplifier," 10th IEEE International Conf. on Electronic, Circuit and System, 2003, (4 pages)
14. **S. Ardalan**, F. Yuan, K. Raahemifar, "Low-Power Technique for Delay Reduction in Static CMOS Circuits," IEEE Northeast Workshop on Circuit and System, 2003, (4 pages)
15. **S. Ardalan**, K. Raahemifar, F. Yuan, "A 1.2V, 8-bit, 100MSample/sec Pipelined Analog-to-Digital Converter," IEEE Northeast Workshop on Circuit and System, 2003, (4 pages)
16. **S. Ardalan**, F. Yuan, K. Raahemifar, "Delay Reduction in Static CMOS Circuits," 16th IEEE European Conference on Circuit Theory and Design, 2003, (4 pages)
17. **S. Ardalan**, K. Raahemifar, F. Yuan, V.Geurkov, "Reed Solomon Encoder & Decoder Design, Simulation and Synthesis," IEEE Canadian Conf. on Elec. and Computer Eng., 2003, (4 pages)
18. **S. Ardalan**, K. Raahemifar, F. Yuan, "Low Voltage Cascode Amplifier," 45th IEEE Mid-West Symposium on Circuit and System, 2002, (4 pages)
19. **S. Ardalan**, S. Krishnan, K. Raahemifar, F. Yuan, "Behavioural Synthesis-able Floating Point Matrix (3x3) Multiplier," IEEE International Conf. for Upcoming Eng., 2002, (4 pages)

Awards

- NSERC Post Doctorial Fellowship (PDF), $80000 (declined) 2010-2011
  - National Sciences and Engineering Research Council of Canada

- NSERC Postgraduate Doctorial Scholarship (PGS-D), $63000 2004-2007
  - National Sciences and Engineering Research Council of Canada

- Graduate Incentive Award, $30000 2004-2007
  - University of Waterloo, Waterloo, Canada

- Strategic Microelectronics Council of ITAC Industrial Award, $3000 2005
  - Information Technology Association of Canada, Strategic Microelectronics Council, Canada

- Ontario Graduate Scholarship, $15000 (declined) 2004
  - Ministry of Training, Colleges and Universities, Ontario, Canada

- Best Paper Award 2004
  - IEEE International Conference for Up-Coming Engineer, Toronto, Canada

- Graduate School Scholarship, $6000 2002
  - Ryerson University, Toronto, Canada

- Best Project Award / Gold Medal 2000
  - Amirkabir University, Tehran, Iran

Professional Activities

- Member of IEEE Region-7 board since 2004
- IEEE Area Chair, 2012
- Chair, IEEE Kitchener/Waterloo Section, 2007, 2008, 2010
- Chair, IEEE Solid-State Circuit Society, Kitchener/Waterloo Section
- Technical Reviewer for JSSCC, ISCAS, MWSCAS, ICUE and potential magazine
- General Co-Chair, IEEE Electrical Power and Energy Conference (EPEC), 2012
- Publicity Chair, IEEE 2010, 11, 12 International Conference On Autonomous and Intelligent Systems (AIS)
- Symposium Co-Chair, the 25th IEEE Canadian Conference on Electronic and Computer Engineering, 2011
- Member of organizing committee for the 24th IEEE Canadian Conference on Electronic and Computer Engineering, 2010
- General Chair and Member of organizing committee for IEEE International Conference for Upcoming Engineers 2009
- Publicity Chair, 2009 IEEE Toronto International Conference Science and Technology for Humanity (TIC-STH 2009)
- Member of technical program committee (Circuits, Devices, and Systems Symposium co-chair) for the 22nd IEEE Canadian Conference on Electronic and Computer Engineering, 2009
- Member of organizing committee for the 21st IEEE Canadian Conference on Electronic and Computer Engineering, 2008
- Student Program Co Chair for IEEE International Conference on System, Man, and Cybernetics, 2007
- General Chair for IEEE International Conference for Upcoming Engineers 2006

Experience

Assistant Professor **2011-Present**

San Jose State University, EE Department, San Jose, USA

- Director of Analog Mixed Signal Centre
- Teaching analog mixed signal related courses for graduate studies.
- Research on
  - high speed wrieline data communication
  - biomedical implantable telemetry circuit
  - robust crypto-processor

Analog Mixed Signal Designer, R&D **2007-2011**

Gennum Corp, Burlington, Canada

- GN2412 Reference-free CDR architecture
  - Member of design and system level modeling for 5 to 15Gbps reference less SerDes.
- GX3288: 288x288 crosspoint analog switch
  - Member of design and verification team for to be the largest analog data switch in the market (288x288).
- High speed bi-directional, multi supply level IO circuit
  - Designing circuit and generating the lib files for a bi-directional digital IO circuit for 2.5V to 1.2V supply voltage which operates in 400MHz speed and robustness of 2KV HBM model for ESD stress.
- GS2994: 2.5V supply, fully blind equalizer for SD/HD/3G SDI application.
  - System level modeling for boost circuits using MATLAB and simulink

  - A novel design and verification for BiCMOS 2.5V core (boosting) block.
- GN1406: Quad Multi-rate Repeater / Re-timer, 2.5Gbps to 6.25Gbps
  - Design and comparison between different architectures for LOS block.

Research Assistant, member of circuit design and reliability research group **2003-2007**
E&CE Department, University of Waterloo, Waterloo, Canada

- Low power, high speed, clock and data recovery
- Biomedical implantable telemeter

Analog CMOS Specialist, R&D, internship **2006-2006**
Dalsa Corp, Waterloo, Canada

- 40MP CMOS Imager
  - Member of design and verification team, responsible for design of analog read out circuitry and noise analysis

Research Assistant, member of microelectronic circuits and systems research group **2002-2003**
E&CE Department, Ryerson University, Toronto, Canada

- Low voltage pipelined analog to digital converter

Biomedical-System Engineer **1999- 2001**
Agfa-Gevaert Inc., Healthcare Department, Tehran, Iran

- Test and design of number of different control board